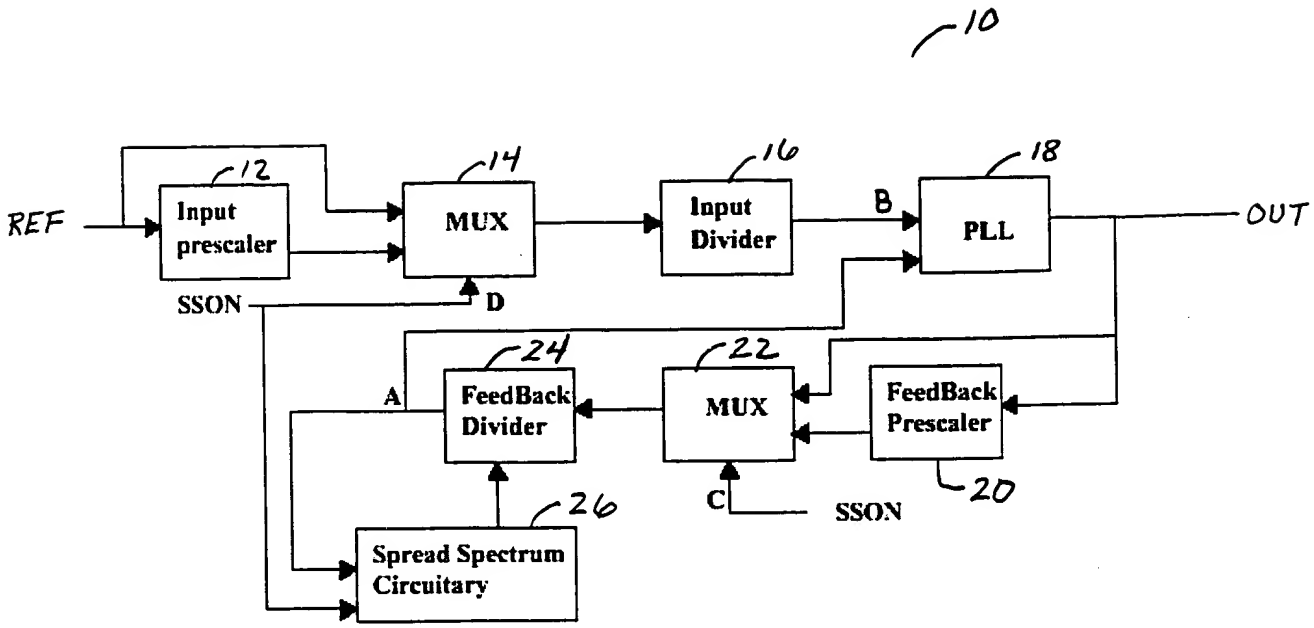
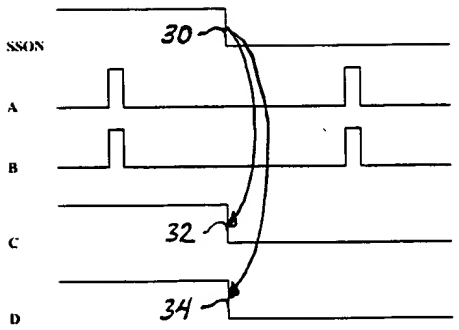

10
REF
12
Input prescaler
14
MUX
16
Input Divider
B
18
PLL
OUT
SSON
D
24
A
FeedBack Divider
22
MUX
FeedBack Prescaler
20
C
SSON
26
Spread Spectrum Circuitary

FIG.1


SSON
30
A
B
C
32
D
34

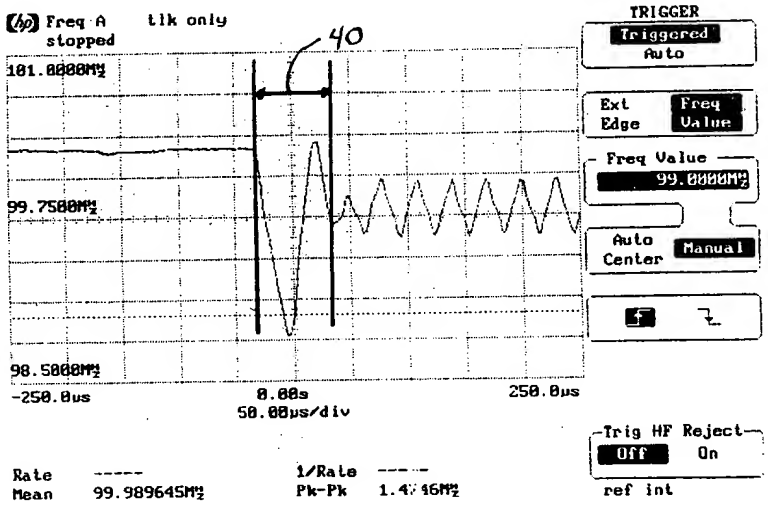

Freq A
stopped
tlk only
40
101.0000MHz
99.7500MHz
98.5000MHz
-250.0us
0.00s
250.0us
50.00us/div
TRIGGER
Triggered
Auto
Ext Edge
Freq Value
Freq Value
99.0000MHz
Auto Center
Manual
Trig HF Reject
Off
On
ref int
Rate
Mean
99.989645MHz
1/Rate
Pk-Pk

FIG. 2

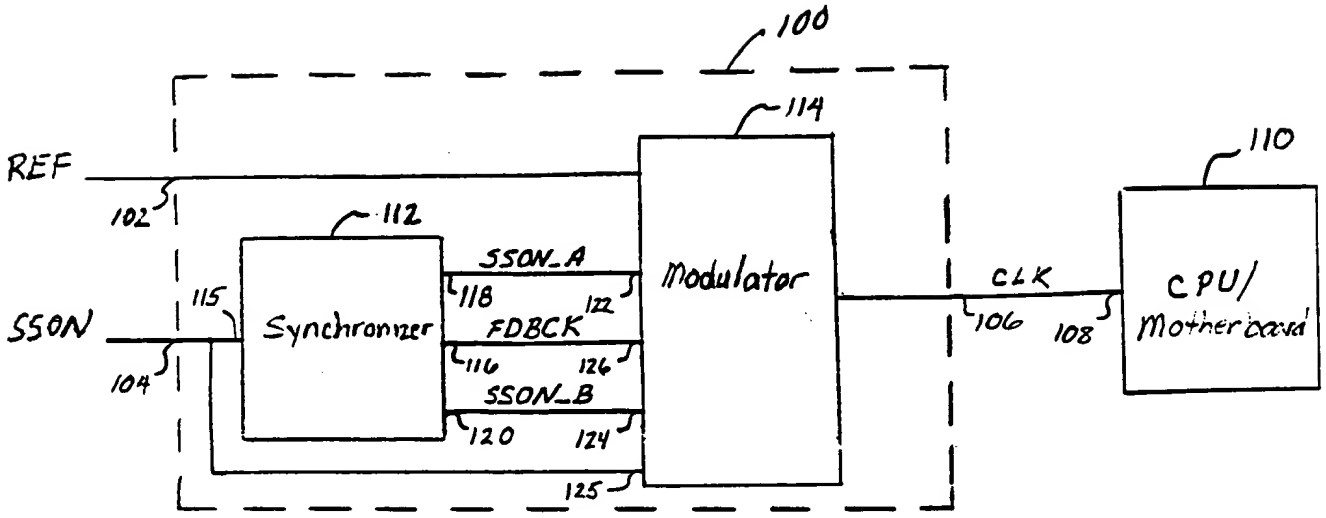

100
114
110
REF
102
112
SSON_A
118
122
Modulator
CLK
CPU/
Motherboard
SSON
115
Synchronizer
FDBCK
116
126
104
SSON_B
120
124
106
108
125

FIG.3

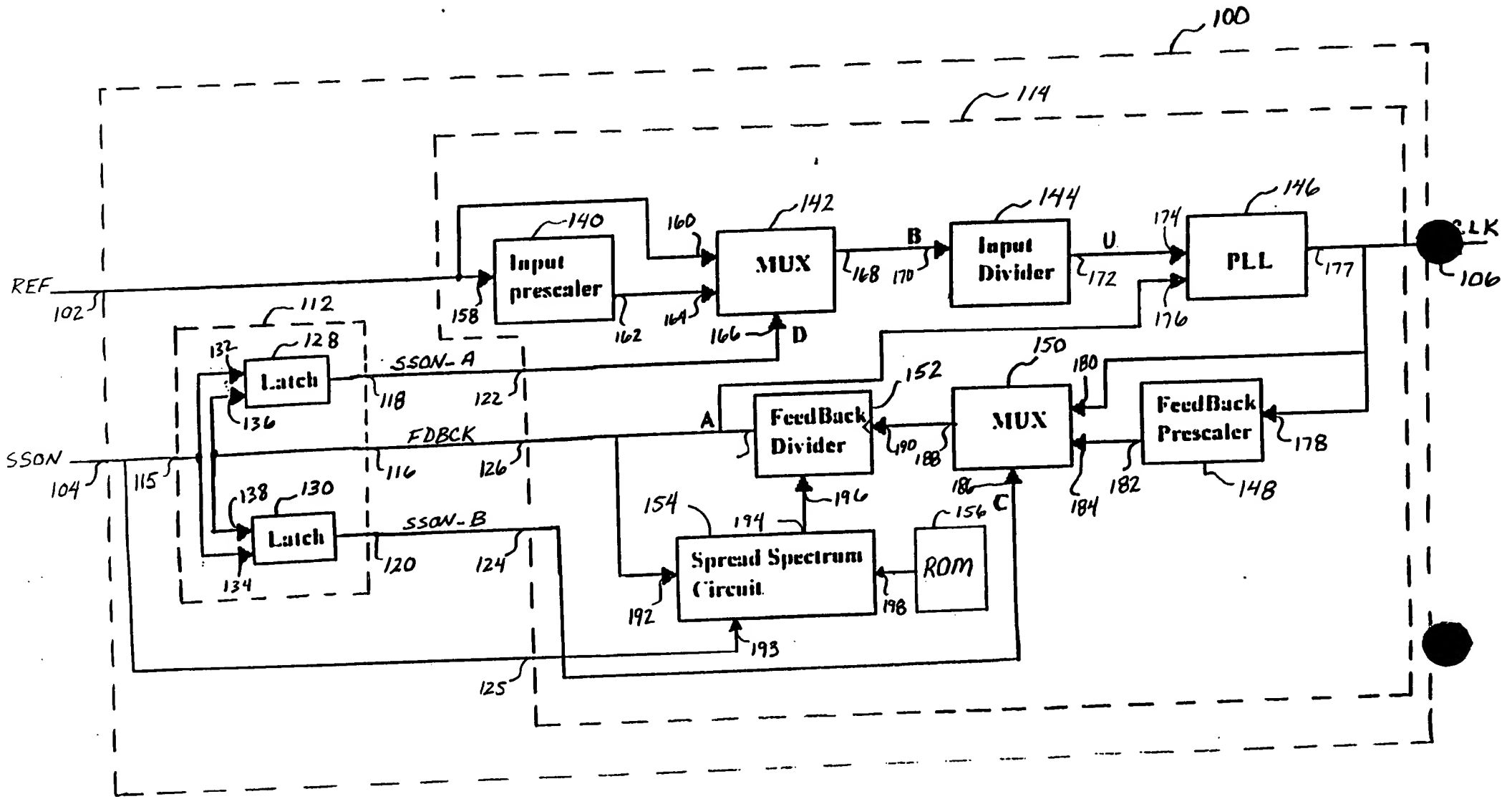

100
114
REF
102
112
158
Input prescaler
140
160
MUX
142
168
170
B
Input Divider
144
172
U
174
PLL
146
177
CLK
106
162
164
166
D
176
132
128
Latch
SSON-A
118
122
136
FDBCK
116
126
SSON
104
115
138
130
Latch
SSON-B
120
124
134
A
FeedBack Divider
152
190
188
MUX
150
180
FeedBack Prescaler
178
182
184
186
C
148
154
194
196
Spread Spectrum Circuit
156
ROM
192
198
193
125

FIG.4

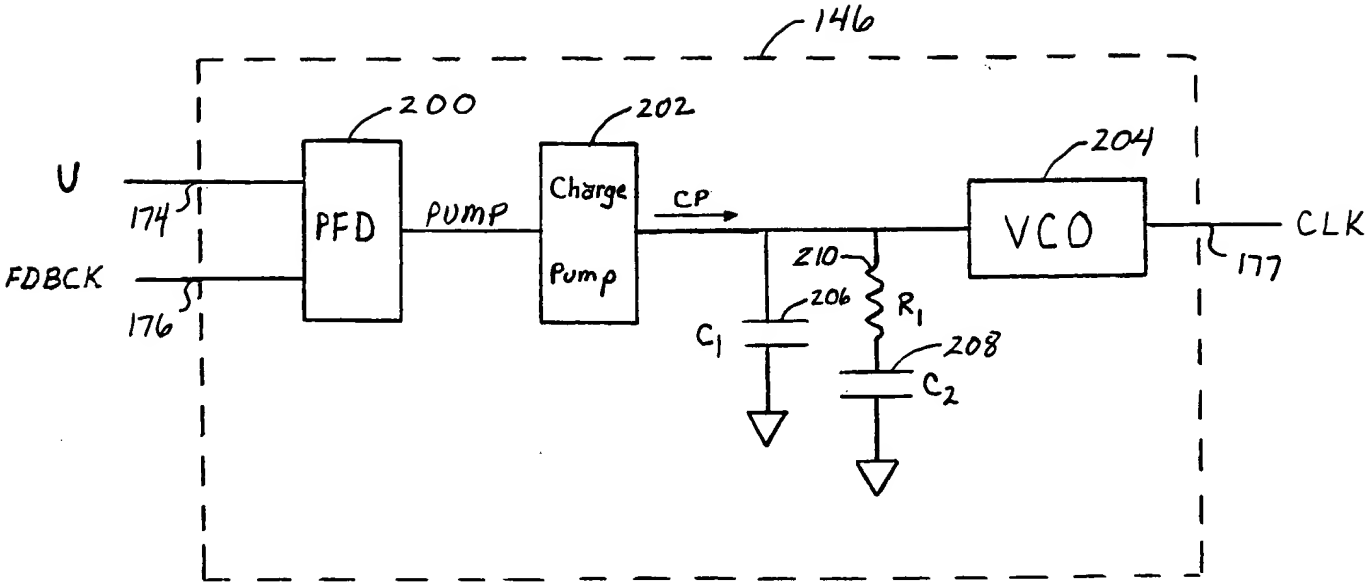
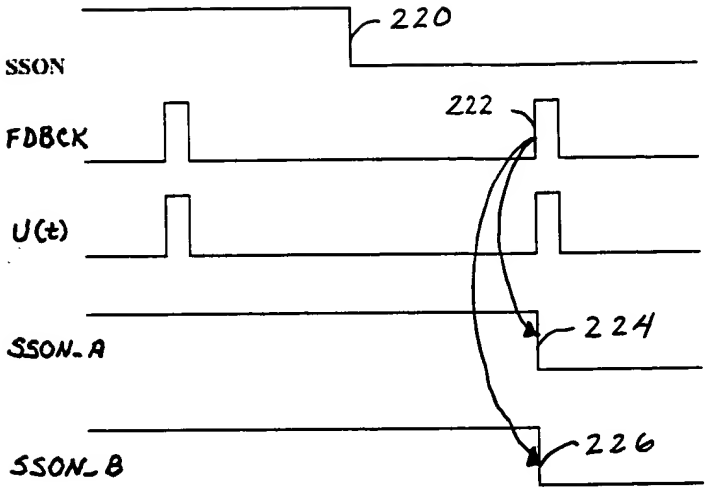
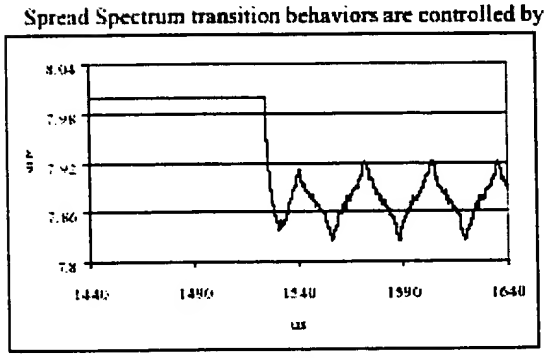

146
200
202
204
U
174
FDBCK
176
PFD
PUMP
Charge
Pump
CP
VCO
CLK
177
210
206
R_1
208
C_1
C_2

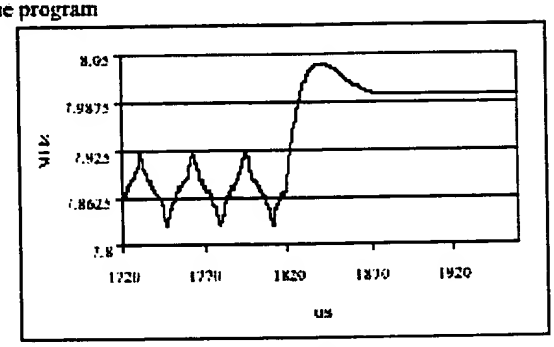
FIG.5



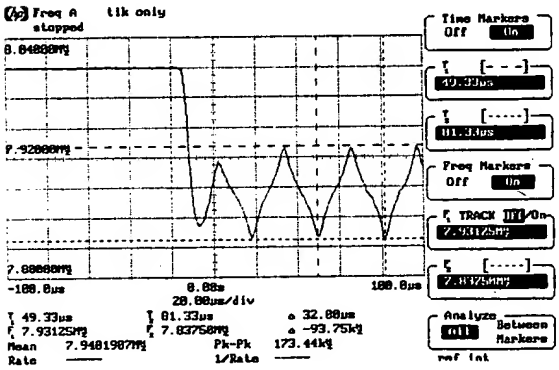
Spread Spectrum transition behaviors are controlled by the program



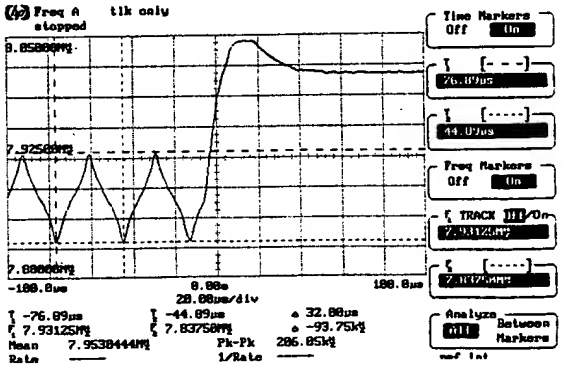
(a)



(a)



(b)



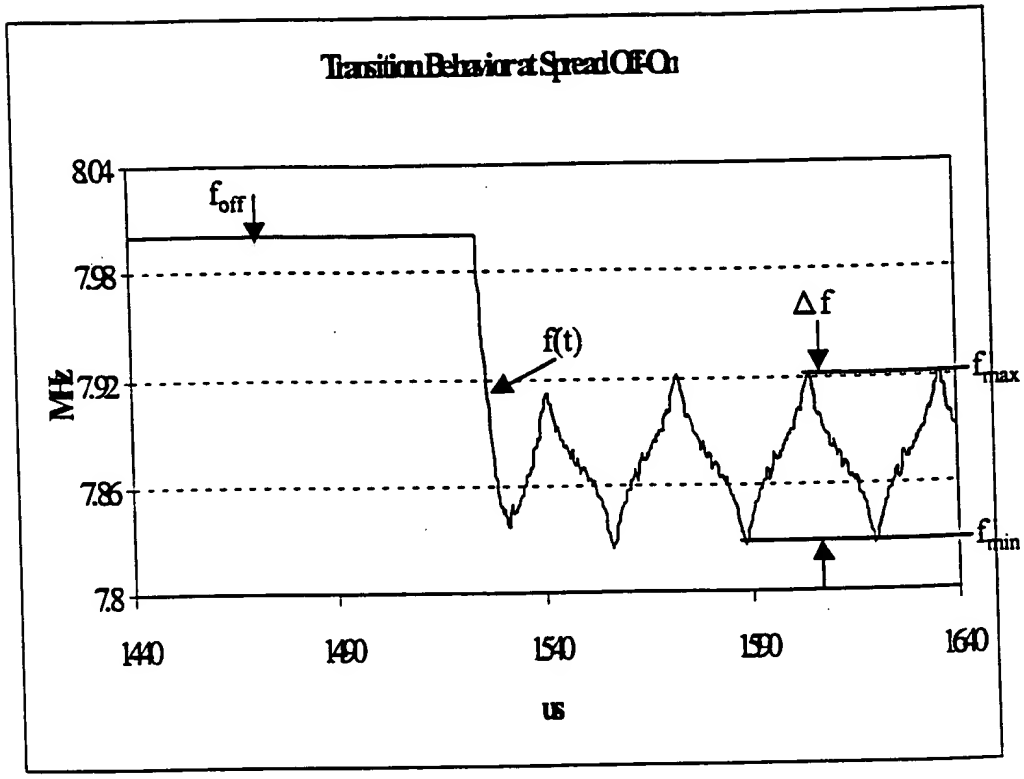
(b)

(a) Simulation (b) Measured results in off-on transition

(a) Simulation (b) Measured results in on-off transition

FIG. 6

Criteria for determining "good and bad" SS transient behavior



f(t): PLL's running frequency in transient period

f_{off}: PLL's SSCG off frequency

f_{max}: Maximum frequency in SSCG on

f_{min}: Minimum frequency in SSCG on

Δ f: Peak to peak frequency in SSCG

Criteria need to be satisfied:

Frequency running range during transient $f_{min} \leq f(t) \leq f_{off}$

FIG.7

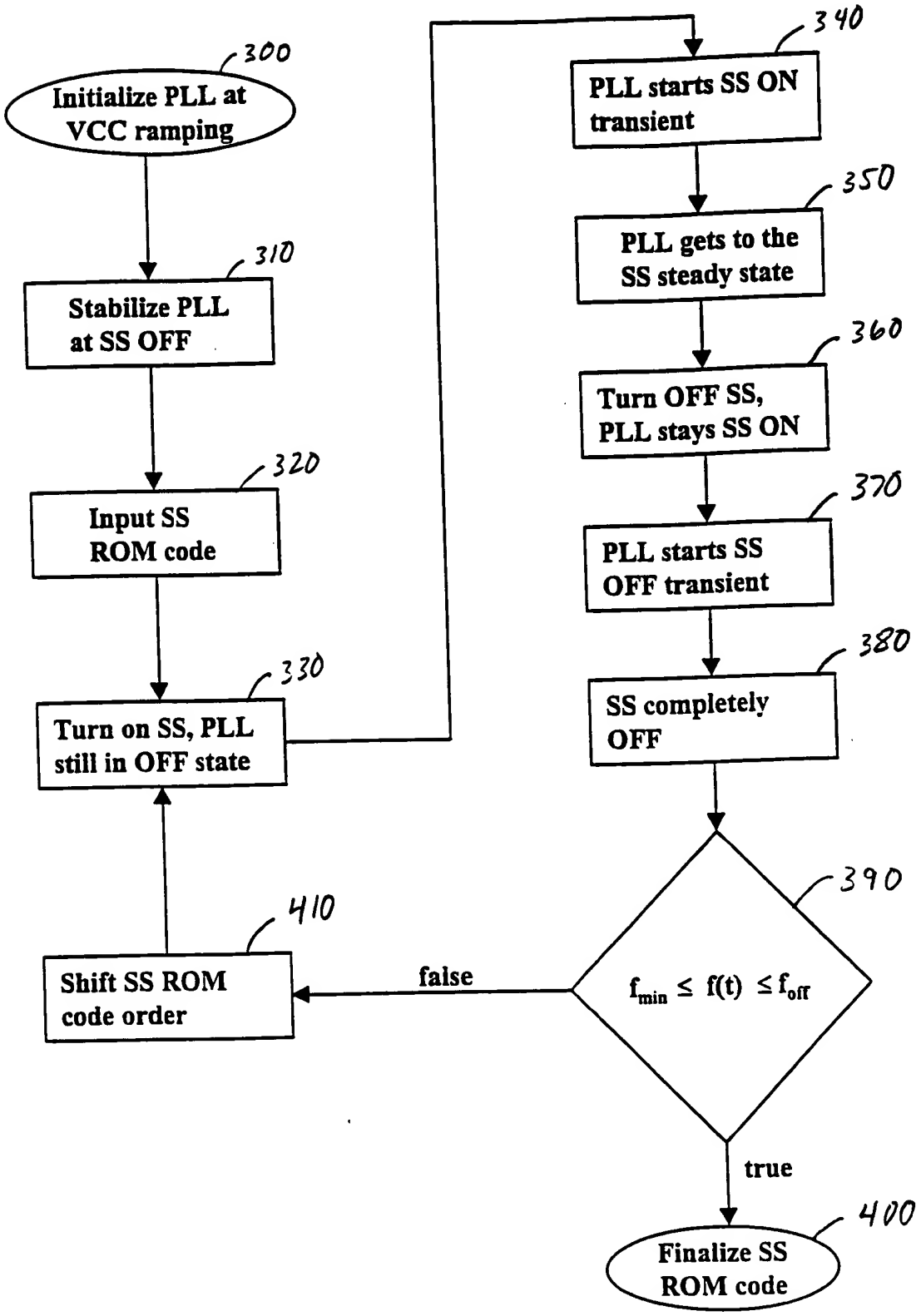
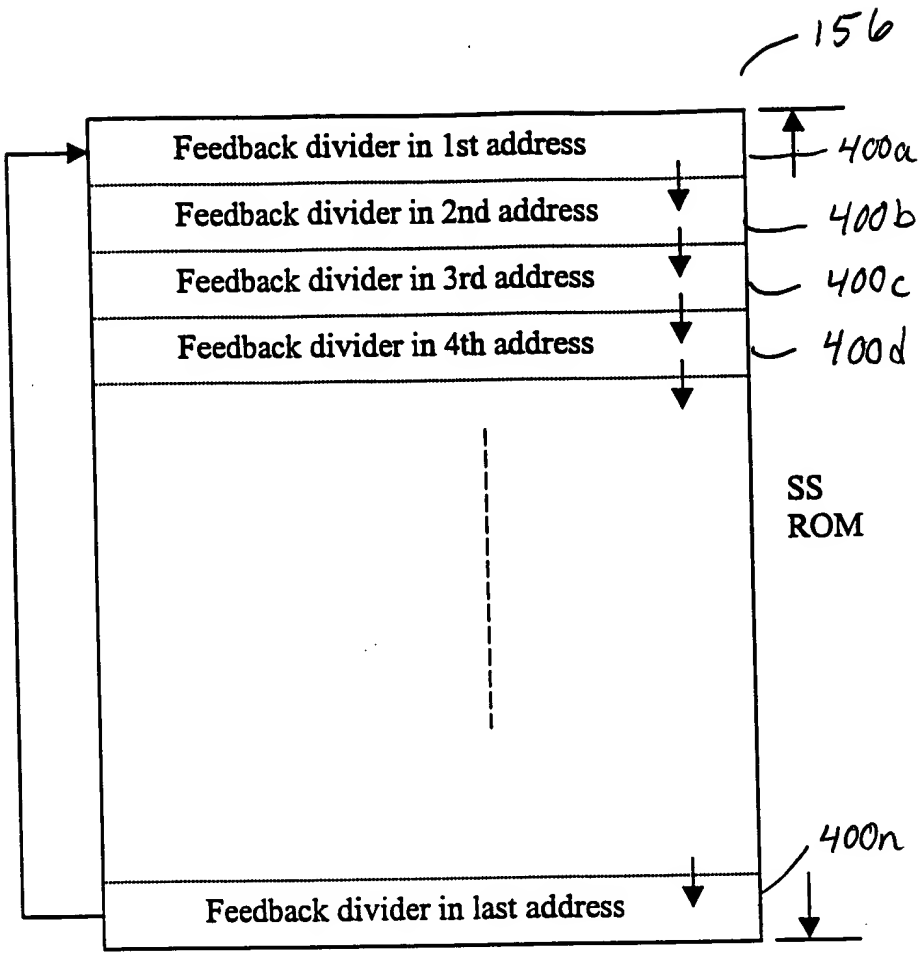

300
Initialize PLL at VCC ramping
310
Stabilize PLL at SS OFF
320
Input SS ROM code
330
Turn on SS, PLL still in OFF state
340
PLL starts SS ON transient
350
PLL gets to the SS steady state
360
Turn OFF SS, PLL stays SS ON
370
PLL starts SS OFF transient
380
SS completely OFF
390
$f_{min} \leq f(t) \leq f_{off}$
false
410
Shift SS ROM code order
true
400
Finalize SS ROM code

FIG.8

Order shifting step in response to bad behavior



Move feedback divider in last address to 1st address and shift down SS ROM code.

FIG.9